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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,766	11/03/2003	Albert Sun	P900383	4242

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
04/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,766	SUN ET AL.	
	Examiner	Art Unit	
	HETUL PATEL	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-15,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-15,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 27, 2008 has been entered and carefully considered.

2. The declaration filed on March 27, 2008 under 37 CFR 1.131 has been considered but is ineffective to overcome the Ikeda et al. (USPN: 2003/0184339) reference because it does not establish conception, reduction to practice, or diligence onto constructive reduction to practice.

3. The rejection of claims 1-10, 13-15 and 18-19 as in the Office Action mailed December 26, 2007 is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 4-6, 8, 14-15 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda et al. (USPN: 2003/0184339) hereinafter, Ikeda.

As per claim 1, Ikeda teaches an integrated circuit (i.e. the system LSI 10 in Fig. 1) comprising: a configurable logic array (i.e. the Offchip FPGA 14 in Fig. 1) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array; a programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1), adapted to store the configuration data; memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; the memory (i.e. the ROM 3 in Fig. 1) being protected from overwriting or modification by an in circuit programming function i.e. ROM is known to have a built-in function which prevents any modification/overwriting of data stored in it) and storing instructions for a configuration load backup function used to recover from an incomplete transfer of the configuration data from the programmable non-volatile configuration memory to the programmable configuration points within the configurable logic array (i.e. the ROM 3 of the processor 11 in Fig. 1 stores the execution program (object program) (similar to BIOS) which can be re-run incase of the incomplete transfer of data; see paragraph [0052]); and a

processor (i.e. the RISC processor 11 in Fig. 1) coupled to the memory which fetches and executes said instructions from the memory (e.g. see paragraphs [0051]-[0052] and Fig. 1).

As per claims 2 and 4, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) comprises a nonvolatile read-only memory (i.e. the ROM) (e.g. see Fig. 1).

As per claims 5 and 6, Ikeda teaches the claimed invention as described above. In order to load/receive data from external device(s) and transferring the data within the FPGA, the load function/instruction and the transfer function/instruction has to be stored in the memory so the processor can execute/run it.

As per claim 8, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the configuration function includes loading the programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) via an input port (i.e. shown in Fig. 1 connecting device 2 and 15) on the integrated circuit (e.g. see Fig. 1).

As per claims 14 and 15, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the integrated circuit further comprises an interface (i.e. the combination of 17, 18, 20 and 21 in Fig. 1) between the processor (i.e. 11 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the configuration function, which loads the programmable non-volatile configuration memory via an input port (i.e. shown in Fig. 1 connecting device 2 and 15) on the integrated

circuit (e.g. see Fig. 1); and an interface (i.e. the combination of 17, 18, 20 and 21 in Fig. 1) between the configuration memory (i.e. 3 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the transfer of configuration data to the configuration logic array (i.e. 14 in Fig. 1) (e.g. see Fig. 1).

As per claims 18 and 19, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the interface between the programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) and the configuration logic array comprises a dedicated data path (i.e. via 17, 20 and 21 in Fig. 1) including the processor (i.e. 11 in Fig. 1) for said transfer of configuration data to the programmable logic array (i.e. 14 in Fig. 1) (e.g. see Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Wirtz, II et al. (USPN: 6,414,871) hereinafter, Wirtz.

As per claim 1, Wirtz teaches a system (i.e. the system shown in Fig. 2) comprising: a configurable logic array (i.e. the 24 in Fig. 2) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array; a programmable non-volatile

configuration memory (i.e. 22 in Fig. 1), adapted to store the configuration data; memory (i.e. the ROM of Host 12 not shown in Fig. 2; it is inherently taught since the host CPU has to have the program memory such as ROM to get the instructions from) storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; and a processor (i.e. the host 12 in Fig. 1) coupled to the memory which fetches and executes said instructions from the memory (e.g. see Col. 8, lines 12+ and Fig. 2).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Hsu et al. (USPN: 5,359,570) hereinafter, Hsu.

As per claim 3, Ikeda teaches that the memory comprises a nonvolatile read-only memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1). However, Ikeda does not teach that the memory comprises a floating gate memory device. Hsu, on the other hand, teaches that floating gate memory devices have the advantage over using the ROM that they can be programmed and erased, electrically, thereby, exhibiting the advantages of ROM memory, i.e., low power consumption and faster access, along with the writeability of magnetic medium. In addition, as integrated circuit fabrication scale increases, greater density can be achieved. Therefore, it would have been obvious to combine Hsu and Ikeda for the benefits described above.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 6,401,221) hereinafter, Sun.

As per claim 7, Ikeda teaches that the claimed invention as described above, but failed to teach the watchdog timer as claimed. Sun, however, discloses a watchdog timer coupled to the CPU (i.e. 122 in Fig. 1), a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function (column 4, lines 15-19). Ikeda and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a watchdog timer and the functions that come with the timer. The suggestion for doing so would have been the ability to reset the system when an error occurs. Therefore, it would have been obvious to combine Sun and Ikeda for the benefit of resetting the system to obtain the invention as specified in claim 7.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 5,901,330) hereinafter, Sun2.

As per claim 9, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration function includes receiving encrypted configuration data via an input port on the integrated circuit, and decrypting the configuration data. Sun2, however, discloses that the configuration function includes receiving encrypted

configuration data via the input port and then decrypting the configuration data (column 13, lines 59-66). Ikeda and Sun2 are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to encrypt the incoming data and then decrypt the data. The suggestion for doing so would have been system security. Therefore, it would have been obvious to combine Sun2 and Ikeda for the benefit of security to obtain the invention as specified in claim 9. The examiner notes that the in-circuit programming and the configuration function perform the same function and are therefore not dissimilar enough to differentiate given the known definitions of the two terms.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Lawman (USPN: 6,028,445).

As per claim 10, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration function includes receiving compressed configuration data via an input port on the integrated circuit, and uncompressing the configuration data. Lawman, however, discloses a configuration function that includes receiving compressed configuration data via an input port and then decompressing the data (column 8, lines 12-33). Ikeda and Lawman are analogous ad because both deal with downloading data in a compressed format to a programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow

the configuration function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and bandwidth. Therefore, it would have been obvious to combine Lawman and Ikeda for the benefit of time and bandwidth savings to obtain the invention as specified in claim 10.

10. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda.

As per claims 11-13, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the programmable configuration memory comprise floating gate memory cells, i.e. charge programmable memory cells (i.e. the FPGA10 in Fig. 17). However, Ikeda does not clarify whether these cells are volatile or not. However, it is well-known and notorious old in the art at the time the current invention was made to combine both the volatile and nonvolatile cells in the FPGA memory. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

Remarks

11. As clearly recited in the interview summary, Examiner never mentioned to Attorney, during any of the multiple phone conversations held on March 25, 2008, that he (Examiner) has opened and reviewed the declaration filed under 1.131. Instead, Examiner clarified to Attorney that he had not and will not open and review the

declaration filed on 02/25/2008 because it was not timely/properly filed (i.e. Applicants have not provided a showing of good and sufficient reasons why the affidavit was not earlier presented) as per MPEP. Examiner also told Attorney that the 131 affidavit/declaration will be entered upon filing RCE; and suggested to make sure 1.131 affidavit/declaration meets all the requirements according to MPEP.

12. The declaration filed on March 27, 2008 under 37 CFR 1.131 has been considered but is ineffective to overcome the Ikeda et al. (USPN: 2003/0184339) reference because it does not establish conception, reduction to practice, or diligence onto constructive reduction to practice.

13. As a preliminary matter, it is unclear whether

- applicants are alleging that a reduction to practice occurred prior to May 24, 2002 (the date of the Ikeda et al. reference); or
- applicants are relying on constructive reduction to practice based on the filing of the application.

14. Both scenarios will be addressed below:

CONCEPTION

15. A conception of an invention, though evidenced by disclosure, drawings, and even a model, is not a complete invention under the patent laws, and confers no rights on an inventor, and has no effect on a subsequently granted patent to another, UNLESS THE INVENTOR FOLLOWS IT WITH REASONABLE DILIGENCE BY SOME OTHER ACT, such as an actual reduction to practice or filing an application for a patent. Automatic Weighing Mach. Co. v. Pneumatic Scale Corp., 166 F.2d 288, 1909 C.D.

498, 139 O.G. 991 (1st Cir. 1909). Conception is the mental part of the inventive act, but it must be capable of proof, as by drawings, complete disclosure to another person, etc. In Mergenthaler v. Scudder, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897), it was established that conception is more than a mere vague idea of how to solve a problem; the means themselves and their interaction must be comprehended also.

The affidavit or declaration and exhibits must clearly explain which facts or data applicant is relying on to show completion of his or her invention prior to the particular date. Vague and general statements in broad terms about what the exhibits describe along with a general assertion that the exhibits describe a reduction to practice "amounts essentially to mere pleading, unsupported by proof or a showing of facts" and, thus, does not satisfy the requirements of 37 CFR 1.131(b). In re Borkowski, 505 F.2d 713, 184 USPQ 29 (CCPA 1974). Applicant must give a clear explanation of the exhibits pointing out exactly what facts are established and relied on by applicant.

16. In the third paragraph of the declaration, applicants allege conception and states that the attached Exhibit supports such conception. This amounts to a vague and general assertion. Applicants have not given a clear explanation of the exhibits pointing out exactly what facts are established and relied on by applicant.

17. There is no explanation of how claims are supported by the disclosed documents. The examiner has reviewed the Exhibit provided and does not find that it supports conception of the claimed invention.

REDUCTION TO PRACTICE

18. Assuming that applicants are relying on a reduction to practice prior to May 24, 2002 (cited reference date), the affidavit is not sufficient. No evidence of reduction to practice has been provided.

NOTE: In general, proof of actual reduction to practice requires a showing that the apparatus actually existed and worked for its intended purpose.

DILIGENCE

19. The following describes the diligence.

In determining the sufficiency of a 37 CFR 1.131 affidavit or declaration, diligence need not be considered unless conception of the invention prior to the effective date is clearly established, since diligence comes into question only after prior conception is established. Ex parte Kantor, 177 USPQ 455 (Bd. App. 1958).

In the interest of compact prosecution, Examiner makes some comments about what is necessary to prove diligence.

Under 37 CFR 1.131, the critical period in which diligence must be shown begins just prior to the effective date of the reference or activity and ends with the date of a reduction to practice, either actual or constructive (i.e., filing a United States patent application).

Mere statements that applicant was diligent without an evidentiary showing is not sufficient.

The period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses. Rebstock v. Flouret, 191 USPQ 342, 345 (Bd. Pat. Inter. 1975).

An applicant must account for the entire period during which diligence is required. Gould v. Schawlow, 363 F.2d 908, 919, 150 USPQ 634, 643 (CCPA 1966) (Merely stating that there were no weeks or months that the invention was not worked on is not enough.); In re Harry, 333 F.2d 920, 923, 142 USPQ 164, 166 (CCPA 1964) (statement that the subject matter "was diligently reduced to practice" is not a showing but a mere pleading).

20. Applicants have not given any evidence(s) of diligence for the period starting from the date of conception (which is not specified but is prior to May 24, 2002 as alleged in the declaration paragraph 4) up until the filing date of the current application, November 03, 2003. Therefore, diligence has not been shown.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- The patent of US application no: 09/875,599 which is allowed/patented but not published yet, teaches the claimed invention, i.e. a flash memory within an IC which loads data from an external memory to an internal memory and a processor within the IC executes the instruction from the internal memory.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2186